REMARKS

Claims 1, 2, and 4-10 are presently pending and stand rejected.

Claims 1, 2, and 4 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Fimoff in view of Yuan.

Claim 1 is amended to recite, among other limitations, "a frame buffer for storing past and future reference pictures" and "said pixel reconstructor further comprising: a macroblock input buffer for storing the reference pixels that are fetched from a frame buffer by the video request manager at the addresses calculated by the motion vector address computer; and a register for storing a portion of the reference pixels that are fetched from the frame buffer by the video request manager at the addresses calculated by the motion vector address computer" and "wherein the register, macroblock input buffer, and frame buffers are separate".

Assignee respectfully submits that Yuan and Fimoff do not teach the foregoing. Examiner has previously indicated that Yuan and Fimoff "as a whole further teaches wherein pixel reconstructor (Yuan, fig. 8, 800) comprises: a macroblock input buffer for storing the reference pixels (Yuan; fig. 8, 801 frame input buffer. Further, the frame input buffer stores both past and future reference frames, which contain reference pixels); and a register for storing a portion of the reference pixel (Yuan, fig. 8, 801. The frame buffer stores both past and future reference frames, which would inherently contain reference pixels)", Previous Office Action, at 5.

It is noted that Examiner reads the "macroblock input buffer for storing the reference pixels that are fetched from a frame buffer" and the "register for storing a portion of the reference pixels that are fetched from the frame buffer" onto Yuan, frame buffer 801. Assignee has amended claim 1 to recite, among other limitations "a frame buffer for storing past and future reference pictures", and "wherein the register, macroblock input buffer, and frame buffers are separate"

Clearly the Yuan, frame buffer 801 cannot be the claimed "macroblock input buffer", "register", and "frame buffer" if the foregoing *are separate*. Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claim 1, 2, and 4.

Secondly, Yuan was filed on Aug. 6, 2004, after the present application. Although Yuan claims priority to provisional patent applications, 60/499,223, 60/493,508, and 60/493,509.

"For prior art purposes, a U.S. patent or patent application publication that claims the benefit of an earlier filing date under 35 U.S.C. **120** of a prior nonprovisional application would be accorded the earlier filing date as its prior art date under 35 U.S.C. **102** (e), provided the earlier-filed application properly supports the subject matter relied upon in any rejection in compliance with 35 U.S.C. **112**, first paragraph. In other words, the subject matter used in the rejection must be disclosed in the earlier-filed application in compliance with 35 U.S.C. **112**, first paragraph, in order for that subject matter to be entitled to the earlier filing date under 35 U.S.C. **102**(e)." MPEP 2136.03.IV.

Assignee respectfully submits that the portions that

are relied on by Examiner, [0037], [0046], [0108], figs. 1, 4, 6, and 8, are not found in the provisional patent applications, 60/499,223, 60/493,508, and 60/493,509. Accordingly, Assignee respectfully traverses the rejection to claims 1-4 because Yuan is not prior art for the claimed invention.

Claims 5-10 were rejected under 35 U.S.C. 103(a) as being obvious from the combination of Diaz in view of Moon and Ueda.

Claim 5 is amended to recite, among other limitations, "a register connected to the multiplexer for storing a portion of the reference pixels that are referenced by the at least one motion vector", Assignee respectfully submits that the registers described in Moon, Figure 3 do not store "a portion of the reference pixels that are referenced by the at least one motion vector".

Moon teaches:

> FIG. 3 includes a first register 300 for storing a bitstream input from the FIFO memory 110, ... and the second register 305 according to the input of a bitstream to be shifted, ... a fifth register 335 for storing zero run-length among outputs from the zero-run & AC decoder 330, ... a sixth register 345 for storing the symbol output from the first multiplexer 340, a second multiplexer 350 for selecting and outputting a bitstream among a variable length bitstream output from the variable length decoder 320, a fixed length bitstream output from the syntax control logic 210, or a 24-bit bitstream which is the largest shift bit number if an escape code of AC exists, a third register 355 for storing a bitstream output from the second multiplexer 350 and inputting a bitstream to be shifted into the shifter 315, a fourth register 360 for storing the effective bits remaining in the second

register 305, a subtracter 365 for subtracting the bitstream of the third register 355 and the effective bits of the fourth register 360...

Emphasis Added.

Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claims 5-10.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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